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EXAMINER	
CUTLER, ALBERT H	
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/679,727	LI ET AL.	
	Examiner	Art Unit	
	Albert H. Cutler	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to application 10/679,727 filed on October 6, 2003. Claims 23-44 are pending in the application and have been examined by the examiner.

Information Disclosure Statement

2. The Information Disclosure Statement (IDS) mailed on March 14, 2005 was received and has been considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 23, 24, and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Rumbaugh(U.S. Patent 6,449,318).

Consider claim 23, Rumbaugh teaches:

A host processor to camera interface(figure 2, column 4, line 10 through column 5, line 60), comprising:

a camera side interface("Transmitter", see top half of figure 2, the camera side

interface can be used to connect a camera, digital video device, etc., column 4, lines 12-30), including:

a camera side link layer("Electronic Device Interface", 100, figure 2) coupled to a camera(column 4, lines 12-30), the camera providing video data(column 4, line 16), the camera side link layer(100) converting the video data to a desired video data format(The camera side link layer converts the input signal into bits(i.e. a desired video data format) which are read into a serial interface, column 4, lines 31-33.);

a serializer("Serial Interface", 101, figure 2) coupled to the camera side link layer(see figure 2) for serializing the video data in the desired video data format(column 4, lines 31-45); and

a camera side transmitter("transceiver", 102, figure 2) coupled to the serializer(see figure 2), the camera side transmitter(102) transmitting the serialized video data(column 4, line 46 through column 5, line 9);

a host processor side interface("Receiver", bottom half of figure 2), including:

a host processor side receiver(The host processor side receiver is comprised of a decoupler(i.e. receiver, 107) which properly receives the transmitted data, column 5, lines 12-19.) for receiving the serialized video data(The decoupler is connected to the twisted pair wiring which carries the incoming serialized data, column 5, lines 12-15);

a deserializer("serial interface buffer", 111, figure 2) coupled to the host processor side receiver(see figure 2, the deserializer(111) is coupled through 108, 109, and 110 to the receiver(107)), the deserializer deserializing the serialized video data(The deserializer provides a converter(i.e. converts the serial data to parallel data)

or a serial bit stream, figure 2, 111.);

and a host processor side link layer("Electronic Device Interface", 112, figure 2) coupled to the deserializer(111) and a host processor(The host processor link layer("digital data interface input device", 112, column 5, lines 34-36) can be used to connect to a computer(i.e. a host processor), column 5, lines 34-36), wherein the host processor side link layer(112) is adapted to convert the deserialized video data into a format compatible with the host processor when required(The host processor side link layer(112) interfaces with a computer(column 5, lines 34-36), and thus inherently converts the video data into a compatible format, as an interface is defined as an arrangement of equipment or programs designed to communicate information from one system of computing devices or programs to another, and enabling separate and sometimes incompatible elements to coordinate effectively.); and

a cable("Twisted Pair Wiring", figure 2) for carrying the video data(column 4, lines 1-9), the cable including a pair of power wires(The cable is a twisted pair copper wire(i.e. a pair of power wires)) for carrying power(column 4, lines 1-9), the cable coupling the camera side transmitter to the host processor side receiver(see figure 2, column 4, line 65 through column 5, line 15).

Consider claim 24, and as applied to claim 23 above, Rumbaugh further teaches that the camera side link layer(100) is configured to convert a plurality of camera video data formats into the desired video format(The electronic device interface(i.e. camera side link layer) interfaces with a multitude of electronic devices(i.e. a plurality of data

formats), some of which provide video data(column 4, lines 16-30), and converts these data formats into bits(i.e. the desired video format) that are read into the serializer, column 4, lines 31-33.).

Consider claim 29, and as applied to claim 23 above, Rumbaugh et al. further teach that the functionality of the host processor side link layer(112) is incorporated within the host processor(The serial interface buffer(111) can be connected directly to a computer(i.e. a host processor) instead of going through a digital data interface(i.e. a link layer), column 5, lines 34-36.).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rumbaugh(U.S. Patent 6,449,318).

Consider claim 25, and as applied to claim 24 above, Rumbaugh teaches that the camera side interface receives a plurality of camera video data formats and converts said video data formats into the desired video format(see claim 24 rationale). Rumbaugh further teaches that a serial interface converter(101) may be necessary when parallel transmission methods are involved, column 4, lines 33-35. Parallel transmission methods mean that a multitude of parallel transmission lines can be used to transmit bits. Rumbaugh does not explicitly teach that the camera video data formats include a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format.

However, **Official Notice** (MPEP § 2144.03) is taken that both the concepts and advantages of having an interface compatible with multiple video data input formats such as a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format are well known and expected in the art. It would have been obvious to a person having ordinary skill in the art at the time of the invention to include an input interface that is compatible with a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format for the benefit of providing a data transmission medium with improved versatility, compatibility, and marketability by accepting multiple bus sizes which transmit many well known video data formats.

8. Claims 26, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rumbaugh in view of Beiley et al.(U.S. Patent 6,522,357), and further in view of Michael(U.S. Patent 4,025,947).

Consider claim 26, and as applied to claim 24 above, Rumbaugh teaches of transmitting video data(see claim 23 rationale) and timing information(column 5, lines 38-61), and of a link layer(see claim 23 rationale).

However, Rumbaugh does not explicitly teach that at least one of the camera video data formats provides a frame valid (FVAL) signal and a line valid (LVAL) signal, and wherein the camera side link layer combines the FVAL signal and the LVAL signal into a single validation (XVAL) signal.

Beiley is similar to Rumbaugh in that an image sensor(408, figure 4) is used to capture an image, and the image sensor communicates serially with a host processor(column 5, lines 49-52).

In addition to the teachings of Rumbaugh, Beiley et al. teach at least one of the camera video data formats provides a frame valid (FVAL) signal and a line valid (LVAL) signal(A frame valid signal is used to indicate valid data for a frame, and a line valid signal is inserted at the start of every row, Column 5, lines 53-60.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have at least one of the camera video data formats provide a frame valid (FVAL) signal and a line valid (LVAL) signal as taught by Beiley et

al. in the data transmission medium taught by Rumbaugh in order to indicate valid data(column 5, lines 53-60) and thus prevent a data loss and discrepancies between an original frame captured by the image sensor and a frame reconstructed by the host processor.

The combination of Rumbaugh and Beiley et al. teaches of providing timing information, and of a frame valid signal and a line valid signal.

However, the combination of Rumbaugh and Beiley et al. does not explicitly teach that the FVAL signal and the LVAL signal are combined into a single validation (XVAL) signal.

Michael is similar to Rumbaugh in that Michael is concerned with transmission of video data(column 3, lines 13-33). Michael is also similar in that a serializer(13, figure 3), and a deserializer(18, figure 3) are used to convert parallel data into serial data for transmission, and serial data into parallel data upon the reception of said transmission(column 3, lines 26-55).

However, in addition to the teachings of Rumbaugh and Beiley et al., Michael teaches of combining multiple signals into a single validation signal(see figure 9, column 6, lines 15-30). In figure 9, under the label "General", Michael teaches a signal envelope indicated by a rectangle with diagonal lines, said envelope contained within a beginning "start" pulse, and an ending "Stop" pulse. Michael further teaches, under the label "Sync", that a synchronization signal is provided parallel to the signal envelope to provide the "start and "stop" pulses. In addition to this, Michael teaches that the signal envelope, and the bit data encloses within it, can be combined with the "Sync" signal to

produce one all-encompassing signal containing both bit-data and timing information(see bottom of figure 9, column 5, line 65 through column 6, line 30).

The signal envelope of Michael is analogous to the frame valid signal of Beiley et al. in that it represents a period in which valid data is contained. That valid data is bit data, as is shown in the bottom of figure 9, and that bit data is analogous to the line valid data of Beiley et al. Therefore, the data pattern shown at the bottom of figure 9, and explained in column 6, lines 15-30, represents a single validation signal which contains a signal envelope(analogous to a the frame valid signal) and a bitstream(analogous to a line valid signal).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to combine the frame valid signal and line valid signal taught by the combination of Rumbaugh and Beiley et al. into one single validation signal as taught by Michael because a single validation signal is the simplest type of signal, and it has the advantage that no synchronization information is required as each piece of data is fully self contained(Michael, column 6, line 23-30).

Consider claim 27, and as applied to claim 26 above, Rumbaugh and Beiley et al. do not explicitly teach that the XVAL signal corresponds to the LVAL signal with and added EOF signal.

However, Michael teaches that the XVAL signal corresponds to the LVAL signal(see figure 9, claim 26 rationale) with and added EOF signal("stop pulse", figure 9, column 6, lines 5-14).

Consider claim 28, and as applied to claim 27 above, Rumbaugh and Beiley et al. do not explicitly teach that a pulse width of the EOF signal is less than the pulse width of the LVAL signal.

However, Michael teaches that a pulse width of the EOF signal is less than the pulse width of the LVAL signal(The LVAL signal taught by Beiley et al. has to be wide enough to indicate the validity of an entire line of data which is composed of a large number of bits. The EOF signal taught by Michael is only one bit long as the signal of Michael comprises a start bit, eight data bits, and a stop bit(i.e. EOF signal, column 6, lines 18-30, see figure 9).

9. Claims 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rumbaugh in view of Tao(U.S. Patent 6,549,239).

Consider claim 30, and as applied to claim 23 above, Rumbaugh teaches a low-voltage differential signaling (LVDS) receiver for serial-to-camera channel communications located within the camera side interface(Rumbaugh teaches of a transceiver(102) located within the camera side interface(see figure 2, column 4, lines 38-49). Rumbaugh teaches that various devices can use the electronic device interface, including low voltage differential signaling(LVDS) devices, column 4, lines 12-26. Therefore, if the interfacing device is an LVDS device, then the receiver must be an

LVDS receiver. Also communication between the camera and host processor is done using a serial interface(i.e. a serial-to-camera channel, column 4, lines 31-45)). Rumbaugh further teaches that an output of the LVDS receiver is coupled to the camera side link layer(see figure 2, the LVDS receiver(102) is coupled to the camera side link layer(100) through the signaling interface(101)).

However, Rumbaugh does not explicitly teach that inputs of the LVDS receiver are coupled to outputs of the camera side transmitter; or

A transmitter for SERTC channel communications located within the host processor side interface, wherein the SERTC channel is provided for reconfiguring the camera, and wherein an input of the LVDS transmitter is coupled to the host processor side link layer and outputs of the LVDS transmitter are coupled to inputs of the host processor side receiver.

Tao is similar to Rumbaugh in that an image sensor(2, figure 2) is used to obtain images, column 4, lines 4-10. Tao is also similar in that an interface bus is used to connect the camera to external devices, column 5, lines 65-67, and said bus is used to transport images and other information, column 6, line 2. Furthermore, Tao is similar in that the bus used to transmit information is a serial bus, column 6, lines 3-15.

However, in addition to the teachings of Rumbaugh, Tao teaches that inputs of the LVDS receiver are coupled to outputs of the camera side transmitter(Tao teaches that the bus is bidirectional, receiving control information and software and parameter updates for the camera, column 5, line 67 through column 6, line 2. Because the bus is bi-directional, the inputs of the LVDS receiver, which receives control information and

software and parameter updates for the camera, are the same as(i.e. coupled to) the outputs of the camera side transmitter).

Tao further teaches a transmitter for SERTC channel communications located within the host processor side interface, wherein the SERTC channel is provided for reconfiguring the camera(Tao teaches that an external device(i.e. host processor) is connected to the camera serially(i.e. SERTC) over a bidirectional bus. That external bus provides(i.e. transmits, thus a transmitter must be contained in the external device) control information and software and parameter updates for the camera(i.e. reconfiguration information), column 5, line 67 through column 6, line 2. Because the SERTC transmitter taught by Tao is sharing the same bus as the host processor side receiver, an input of the transmitter is coupled to the host processor side link layer taught by Rumbaugh due to the fact that the transmitter has to be coupled to the host processor side receiver, which is in turn coupled to the host processor side link layer(see claim 23 rationale). Because the bus taught by Tao is bidirectional, the outputs of the transmitter are the same as(i.e. coupled to) inputs of the host processor side receiver).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to configure the bus taught by Rumbaugh as a bidirectional bus in order provide the camera with control information and software and parameter updates as well as send images to an external device as taught by Tao for the benefit that the bus is simple, low cost, and versatile since the camera can be controlled from a remote location using the host processor(Tao, column 5, line 65 through column 6, line

35).

Consider claim 31, and as applied to claim 30 above, Rumbaugh further teaches that the cable includes a first pair of signal wires for carrying the video data(The cable is a twisted pair(i.e. a first pair of signal wires), column 4, lines 1-9, figure 2. The cable is used for carrying video data, column 4, lines 14-30.), and wherein the video data is in the form of a low-voltage differential signaling (LVDS) data stream(The interfaced device may be a LVDS device(i.e. a device which transmits LVDS data) column 4, line 26).

Consider claim 32, and as applied to claim 31 above, Rumbaugh teaches of a camera side link layer, and a host processor side link layer(see claim 23 rationale). Rumbaugh also teaches of a first pair of wires which communicate video data in the desired format(see claim 31 rationale).

However, Rumbaugh does not explicitly teach that the camera side link layer and the host processor side link layer are configured to share the first pair of signal wires to communicate the video data in the desired video signal format and configuration signals for the SERTC channel.

However, Tao teaches that the camera side and the host processor side are configured to share signal wires to communicate the video data in the desired video signal format and configuration signals for the SERTC channel(Tao teaches of a bidirectional bus(i.e. a shared bus between the camera side and the host processor

side), and that the bus communicates image data and configuration signals for the SERTC channel(column 5, line 67 through column 6, line 2).).

Consider claim 33, and as applied to claim 30 above, Rumbaugh does not explicitly teach that the cable further includes a second pair of signal wires to communicate configuration signals for the SERTC channel.

However, Tao teaches that the cable further includes a second pair of signal wires(Tao teaches that a six-wire shielded cable(i.e. a first, second, and third pair of wires) can be used to achieve high data transmission rates, column 6, lines 7-10) to communicate configuration signals for the SERTC channel(column 5, line 67 through column 6, line 10).

10. Claims 34 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rumbaugh in view of Stam et al.(U.S. Patent Application Publication 2004/0143380).

Consider claim 34, Rumbaugh teaches:

A host processor to camera interface(figure 2, column 4, line 10 through column 5, line 60), comprising:

a camera side interface("Transmitter", see top half of figure 2, the camera side interface can be used to connect a camera, digital video device, etc., column 4, lines 12-30), including:

a camera side link layer("Electronic Device Interface", 100, figure 2) coupled to a camera(column 4, lines 12-30), the camera providing video data(column 4, line 16), the camera side link layer(100) converting the video data to a desired video data format(The camera side link layer converts the input signal into bits(i.e. a desired video data format) which are read into a serial interface, column 4, lines 31-33.);

a serializer("Serial Interface", 101, figure 2) coupled to the camera side link layer(see figure 2) for serializing the video data in the desired video data format(column 4, lines 31-45); and

a camera side transmitter("transceiver", 102, figure 2) coupled to the serializer(see figure 2), the camera side transmitter(102) transmitting the serialized video data(column 4, line 46 through column 5, line 9);

a host processor side interface("Receiver", bottom half of figure 2), including:

a host processor side receiver(The host processor side receiver is comprised of a decoupler(i.e. receiver, 107) which properly receives the transmitted data, column 5, lines 12-19.) for receiving the serialized video data(The decoupler is connected to the twisted pair wiring which carries the incoming serialized data, column 5, lines 12-15);

a deserializer("serial interface buffer", 111, figure 2) coupled to the host processor side receiver(see figure 2, the deserializer(111) is coupled through 108, 109, and 110 to the receiver(107)), the deserializer deserializing the serialized video data(The deserializer provides a converter(i.e. converts the serial data to parallel data) or a serial bit stream, figure 2, 111.);

and a host processor side link layer("Electronic Device Interface", 112, figure 2)

coupled to the deserializer(111) and a host processor(The host processor link layer("digital data interface input device", 112, column 5, lines 34-36)) can be used to connect to a computer(i.e. a host processor), column 5, lines 34-36), wherein the host processor side link layer(112) is adapted to convert the deserialized video data into a format compatible with the host processor when required(The host processor side link layer(112) interfaces with a computer(column 5, lines 34-36), and thus inherently converts the video data into a compatible format, as an interface is defined as an arrangement of equipment or programs designed to communicate information from one system of computing devices or programs to another, and enabling separate and sometimes incompatible elements to coordinate effectively.); and

a cable("Twisted Pair Wiring", figure 2) for carrying the video data(column 4, lines 1-9), the cable including a pair of power wires(The cable is a twisted pair copper wire(i.e. a pair of power wires)) for carrying power(column 4, lines 1-9), the cable coupling the camera side transmitter to the host processor side receiver(see figure 2, column 4, line 65 through column 5, line 15).

However, Rumbaugh does not explicitly teach that the camera is attached to a motor vehicle, or that the host processor is incorporated within an electronic control unit of the motor vehicle that is remote from the camera.

Rumbaugh also does not teach that the camera side link layer is configured to convert a plurality of camera video data formats into the desired video data format, and wherein the camera video data formats include a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit

data format.

Stam et al. is similar to Rumbaugh in that an imager("Pixel array", figure 3) is used to communicate with a host processor, paragraph 0037. Stam et al. is also similar in that and LVDS serial interface is used as the communication medium, paragraph 0037.

However, in addition to the teachings of Rumbaugh, Stam et al. teach that the camera is attached to a motor vehicle(paragraph 0032), and that the host processor is incorporated within an electronic control unit of the motor vehicle that is remote from the camera(The camera can be mounted on a separate structure(i.e. remote from the processor), paragraph 0035, paragraph 0032. The image captured by the camera and transmitted to the processor is analyzed to determine if high beams of the vehicle's headlamps should be shut off or otherwise modified, paragraph 0033. Therefore, the host processor must be incorporated within an electronic control unit of the motor vehicle as the results from the processor are used to electronically control the motor vehicle's headlamps.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to contain the invention of Rumbaugh within a motor vehicle as taught by Stam et al. in order to provide image information used to automatically control vehicle equipment such as exterior lights, windshield wipers, and defrosters, and thus improve driving safety and provide convenience to the driver(Stam et al., paragraphs 0002-0004).

The combination of Rumbaugh and Stam et al. teaches of a camera and host

processor system incorporated in a motor vehicle. However, the combination does not explicitly teach that the camera side link layer is configured to convert a plurality of camera video data formats into the desired video data format, and wherein the camera video data formats include a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format.

However, **Official Notice** (MPEP § 2144.03) is taken that both the concepts and advantages of having an interface compatible with multiple video data input formats such as a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format are well known and expected in the art. It would have been obvious to a person having ordinary skill in the art at the time of the invention to include an input interface that is compatible with a single 8-bit data format, a dual 8-bit data format, a single 16-bit data format, a single 24-bit data format and a single 12-bit data format for the benefit of providing a data transmission medium with improved versatility, compatibility, and marketability by accepting multiple bus sizes which transmit many well known video data formats.

Consider claim 38, and as applied to claim 34 above, Rumbaugh et al. further teach that the functionality of the host processor side link layer(112) is incorporated within the host processor(The serial interface buffer(111) can be connected directly to a computer(i.e. a host processor) instead of going through a digital data interface(i.e. a link layer), column 5, lines 34-36.).

11. Claims 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rumbaugh in view of Stam et al. as applied to claim 34 above, and further in view of Beiley et al.(U.S. Patent 6,522,357), and further in view of Michael(U.S. Patent 4,025,947).

Consider claim 35, and as applied to claim 34 above, Rumbaugh teaches of transmitting video data(see claim 34 rationale) and timing information(column 5, lines 38-61), and of a link layer(see claim 34 rationale).

However, the combination of Rumbaugh and Stam et al. does not explicitly teach that at least one of the camera video data formats provides a frame valid (FVAL) signal and a line valid (LVAL) signal, and wherein the camera side link layer combines the FVAL signal and the LVAL signal into a single validation (XVAL) signal.

Beiley is similar to Rumbaugh in that an image sensor(408, figure 4) is used to capture an image, and the image sensor communicates serially with a host processor(column 5, lines 49-52).

In addition to the teachings of Rumbaugh and Stam et al., Beiley et al. teach at least one of the camera video data formats provides a frame valid (FVAL) signal and a line valid (LVAL) signal(A frame valid signal is used to indicate valid data for a frame, and a line valid signal is inserted at the start of every row, Column 5, lines 53-60.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have at least one of the camera video data formats provide a frame valid (FVAL) signal and a line valid (LVAL) signal as taught by Beiley et

al. in the data transmission medium taught by Rumbaugh in order to indicate valid data(column 5, lines 53-60) and thus prevent a data loss and discrepancies between an original frame captured by the image sensor and a frame reconstructed by the host processor.

The combination of Rumbaugh, Stam et al., and Beiley et al. teaches of providing timing information, and of a frame valid signal and a line valid signal.

However, the combination of Rumbaugh, Stam et al., and Beiley et al. does not explicitly teach that the FVAL signal and the LVAL signal are combined into a single validation (XVAL) signal.

Michael is similar to Rumbaugh in that Michael is concerned with transmission of video data(column 3, lines 13-33). Michael is also similar in that a serializer(13, figure 3), and a deserializer(18, figure 3) are used to convert parallel data into serial data for transmission, and serial data into parallel data upon the reception of said transmission(column 3, lines 26-55).

However, in addition to the teachings of Rumbaugh and Beiley et al., Michael teaches of combining multiple signals into a single validation signal(see figure 9, column 6, lines 15-30). In figure 9, under the label "General", Michael teaches a signal envelope indicated by a rectangle with diagonal lines, said envelope contained within a beginning "start" pulse, and an ending "Stop" pulse. Michael further teaches, under the label "Sync", that a synchronization signal is provided parallel to the signal envelope to provide the "start and "stop" pulses. In addition to this, Michael teaches that the signal envelope, and the bit data encloses within it, can be combined with the "Sync" signal to

produce one all-encompassing signal containing both bit-data and timing information(see bottom of figure 9, column 5, line 65 through column 6, line 30).

The signal envelope of Michael is analogous to the frame valid signal of Beiley et al. in that it represents a period in which valid data is contained. That valid data is bit data, as is shown in the bottom of figure 9, and that bit data is analogous to the line valid data of Beiley et al. Therefore, the data pattern shown at the bottom of figure 9, and explained in column 6, lines 15-30, represents a single validation signal which contains a signal envelope(analogous to a the frame valid signal) and a bitstream(analogous to a line valid signal).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to combine the frame valid signal and line valid signal taught by the combination of Rumbaugh, Stam et al., and Beiley et al. into one single validation signal as taught by Michael because a single validation signal is the simplest type of signal, and it has the advantage that no synchronization information is required as each piece of data is fully self contained(Michael, column 6, line 23-30).

Consider claim 36, and as applied to claim 35 above, Rumbaugh, Stam et al., and Beiley et al. do not explicitly teach that the XVAL signal corresponds to the LVAL signal with and added EOF signal.

However, Michael teaches that the XVAL signal corresponds to the LVAL signal(see figure 9, claim 35 rationale) with and added EOF signal("stop pulse", figure 9, column 6, lines 5-14).

Consider claim 37, and as applied to claim 36 above, Rumbaugh and Beiley et al. do not explicitly teach that a pulse width of the EOF signal is less than the pulse width of the LVAL signal.

However, Michael teaches that a pulse width of the EOF signal is less than the pulse width of the LVAL signal(The LVAL signal taught by Beiley et al. has to be wide enough to indicate the validity of an entire line of data which is composed of a large number of bits. The EOF signal taught by Michael is only one bit long, as the signal of Michael comprises a start bit, eight data bits, and a stop bit(i.e. EOF signal, column 6, lines 18-30, see figure 9).

12. Claims 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rumbaugh in view of Stam et al. as applied to claim 34 above, and further in view of Tao(U.S. Patent 6,549,239).

Consider claim 39, and as applied to claim 34 above, Rumbaugh teaches a low-voltage differential signaling (LVDS) receiver for serial-to-camera channel communications located within the camera side interface(Rumbaugh teaches of a transceiver(102) located within the camera side interface(see figure 2, column 4, lines 38-49). Rumbaugh teaches that various devices can use the electronic device interface, including low voltage differential signaling(LVDS) devices, column 4, lines 12-

26. Therefore, if the interfacing device is an LVDS device, then the receiver must be an LVDS receiver. Also communication between the camera and host processor is done using a serial interface(i.e. a serial-to-camera channel, column 4, lines 31-45)). Rumbaugh further teaches that an output of the LVDS receiver is coupled to the camera side link layer(see figure 2, the LVDS receiver(102) is coupled to the camera side link layer(100) through the signaling interface(101)).

However, the combination of Rumbaugh and Stam et al. does not explicitly teach that inputs of the LVDS receiver are coupled to outputs of the camera side transmitter; and

A transmitter for SERTC channel communications located within the host processor side interface, wherein the SERTC channel is provided for reconfiguring the camera, and wherein an input of the LVDS transmitter is coupled to the host processor side link layer and outputs of the LVDS transmitter are coupled to inputs of the host processor side receiver.

Tao is similar to Rumbaugh in that an image sensor(2, figure 2) is used to obtain images, column 4, lines 4-10. Tao is also similar in that an interface bus is used to connect the camera to external devices, column 5, lines 65-67, and said bus is used to transport images and other information, column 6, line 2. Furthermore, Tao is similar in that the bus used to transmit information is a serial bus, column 6, lines 3-15.

However, in addition to the teachings of Rumbaugh and Stam et al., Tao teaches that inputs of the LVDS receiver are coupled to outputs of the camera side transmitter(Tao teaches that the bus is bidirectional, receiving control information and

software and parameter updates for the camera, column 5, line 67 through column 6, line 2. Because the bus is bi-directional, the inputs of the LVDS receiver, which receives control information and software and parameter updates for the camera, are the same as(i.e. coupled to) the outputs of the camera side transmitter).

Tao further teaches a transmitter for SERTC channel communications located within the host processor side interface, wherein the SERTC channel is provided for reconfiguring the camera(Tao teaches that an external device(i.e. host processor) is connected to the camera serially(i.e. SERTC) over a bidirectional bus. That external bus provides(i.e. transmits, thus a transmitter must be contained in the external device) control information and software and parameter updates for the camera(i.e. reconfiguration information)). Because the SERTC transmitter taught by Tao is sharing the same bus as the host processor side receiver, an input of the transmitter is coupled to the host processor side link layer taught by Rumbaugh due to the fact that the transmitter has to be coupled to the host processor side receiver, which is in turn coupled to the host processor side link layer(see claim 23 rationale). Because the bus taught by Tao is bidirectional, the outputs of the transmitter are the same as(i.e. coupled to) inputs of the host processor side receiver.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to configure the bus taught by the combination of Rumbaugh and Stam et al. as a bidirectional bus in order provide the camera with control information and software and parameter updates as well as send images to an external device as taught by Tao for the benefit that the bus is simple, low cost, and versatile

since the camera can be controlled from a remote location using the host processor(Tao, column 5, line 65 through column 6, line 35).

Consider claim 40, and as applied to claim 39 above, Rumbaugh further teaches that the cable includes a first pair of signal wires for carrying the video data(The cable is a twisted pair(i.e. a first pair of signal wires), column 4, lines 1-9, figure 2. The cable is used for carrying video data, column 4, lines 14-30.), and wherein the video data is in the form of a low-voltage differential signaling (LVDS) data stream(The interfaced device may be a LVDS device(i.e. a device which transmits LVDS data) column 4, line 26).

Consider claim 41, and as applied to claim 40 above, Rumbaugh teaches of a camera side link layer, and a host processor side link layer(see claim 23 rationale). Rumbaugh also teaches of a first pair of wires which communicate video data in the desired format(see claim 31 rationale).

However, the combination of Rumbaugh and Stam et al. does not explicitly teach that the camera side link layer and the host processor side link layer are configured to share the first pair of signal wires to communicate the video data in the desired video signal format and configuration signals for the SERTC channel.

However, Tao teaches that the camera side and the host processor side are configured to share signal wires to communicate the video data in the desired video signal format and configuration signals for the SERTC channel(Tao teaches of a

bidirectional bus(i.e. a shared bus between the camera side and the host processor side), and that the bus communicates image data and configuration signals for the SERTC channel(column 5, line 67 through column 6, line 2).).

Consider claim 42, and as applied to claim 40 above, the combination of Rumbaugh and Stam et al. does not explicitly teach that the cable further includes a second pair of signal wires to communicate configuration signals for the SERTC channel.

However, Tao teaches that the cable further includes a second pair of signal wires(Tao teaches that a six-wire shielded cable(i.e. a first, second, and third pair of wires) can be used to achieve high data transmission rates, column 6, lines 7-10) to communicate configuration signals for the SERTC channel(column 5, line 67 through column 6, line 10).

13. Claims 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bechtel et al.(U.S. Patent 5,990,469) in view of Rumbaugh.

Consider Claim 43, Bechtel et al. teach:

A method for sharing(the interface is bi-directional, column 14, lines 34-37) signal wires(column 14, line 18 through column 17, line 24), comprising the steps of:

providing a trigger pulse from a host processor side to a camera side(The microcontroller(i.e. host processor) provides a "Read" instruction(i.e. trigger pulse) to

the camera column 15, lines 62-64, column 16, lines 11-14.) through a power line(serial communication interface, column 4, lines 32-34, column 14, lines 34-37);

disabling the camera side and enabling a serial-to-camera (SERTC) channel receiver in the camera side in response to receiving the trigger pulse on the power line(The readout function is inhibited(i.e. the camera side transmission from the camera side is disabled) when the a reset function(i.e. reset trigger pulse) is commanded by the microcontroller, column 15, lines 52-55, column 16, lines 5-11. The microcontroller communicates over a serial interface(i.e. SERTC) with the camera and the camera receives "reset" instructions(i.e. a serial-to-camera channel receiver is enabled) through said serial interface, column 15, lines 52-55, column 16, lines 5-11.);

monitoring the status of the signal lines by examining outputs located in the host processor side(The readout of transmitted image data(i.e. the readout of the outputs of the signal lines) at the host processor is monitored by the microcontroller, which disables a reset function until the readout of the image data is completed, column 16, lines 11-14.);

enabling a SERTC channel transmitter located in the host processor side to establish a serial communication interface (SCI) between a camera coupled to the camera side and a host processor coupled to the host processor side via the signal lines when the outputs indicate the signal lines are free(The microcontroller(i.e. host processor) transmits(i.e. a transmitter is enabled) a reset function over the serial interface(i.e. a serial communication interface between the camera coupled to the camera side and a host processor coupled to the host processor side) via the signal

lines when the outputs indicate the signal lines are free(When the readout of the pixels is completed, the signal lines are free, and the microcontroller establishes SERTC communication with the camera and provides the "reset" instruction, column 15, line 52 through column 16, line 14).

However, Bechtel et al. do not explicitly teach that a serializer and deserializer are used, that a link layer is provided on the camera side and on the host processor side, or that the signal lines comprise a pair of lines.

Rumbaugh is similar to Bechtel et al. in that a camera(100, figure 2) communicates with a host processor(112, figure 2) over a serial interface(Video data is transmitted serially over a twisted pair wiring(column 4, lines 1-9). Rumbaugh is also similar in that transmitter is disabled when not transmitting data(column 1, lines 18-35).

However, in addition to the teachings of Bechtel et al., Rumbaugh explicitly teaches of the use of a serializer("Serial Interface", 101, figure 2) and a deserializer("serial interface buffer", 111, figure 2) in the transmission of video data(The camera side link layer converts the input signal into bits(i.e. a desired video data format) which are read into a serial interface, column 4, lines 31-33.). Rumbaugh also teaches that a link layer is provided on the camera side("Electronic Device Interface", 100, figure 2) and on the host processor side("Electronic Device Interface", 112, figure 2). The host processor link layer("digital data interface input device", 112, column 5, lines 34-36) can be used to connect to a computer(i.e. a host processor), column 5, lines 34-36. Rumbaugh further teaches that the signal lines comprise a pair of lines(The cable is a twisted pair copper wire(i.e. a pair of power wires) for carrying power, column 4, lines 1-

9.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to include a serializer and a deserializer, camera side and host processor side link layers, and a twisted pair copper wire as taught by Rumbaugh in the camera/host-processor serial interface taught by Bechtel et al. for the benefit that serializers and deserializers utilized in conjunction with camera side and host processor side link layers create a more versatile device since a multitude of different input and output devices with different configurations can utilize the transmission medium(Rumbaugh, column 4, lines 12-45), and twisted pair copper wire transmission allows high transmission rates, high quality of service, and a low bit error rate(Rumbaugh, column 1, line 50 through column 2, line 10).

Consider claim 44, and as applied to claim 43 above, Bechtel et al. further teach of disabling the serial to camera communication(The reset function(which is provided by serial to camera communication), is inhibited(i.e. disabled), column 15, lines 52-55, column 16, line 11-14.) and enabling the readout of images in response to the reset message(At the end of the reset function(i.e. reset message), images are read out using the "readout" function, column 15, lines 52-55, column 16, lines 11-14), wherein the reset message is provided by the host processor("microcontroller", column 16, line 11) sending a reset signal(column 15, line 55 through column 16, line 14). to the host processor side.

Bechtel et al. do not explicitly teach of a host processor side link layer, a

serializer, or a deserializer. However, Rumbaugh teaches of a host processor side link layer, a serializer, and a deserializer(see claim 43 rationale).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert H. Cutler whose telephone number is (571)-270-1460. The examiner can normally be reached on Mon-Fri (7:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571)-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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